In the Claims:

This listing of claims replaces all prior versions.

1. (Previously Presented) Method of manufacturing a semiconductor device comprising a field effect transistor, in which method a semiconductor body of silicon is provided at a surface thereof with a source region and a drain region of a first conductivity type, which regions are both provided with extensions, and with a channel region of a second conductivity type, opposite to the first conductivity type, between the source region and the drain region, and with a gate region separated from the surface of the semiconductor body by a gate dielectric and situated above the channel region, and wherein a pn-junction between the extensions and a neighboring part of the channel region is formed by two implantations of dopants of opposite conductivity type, and wherein before both of said two implantations of dopants of opposite conductivity type are performed an amorphizing implantation is performed where the pn-junction is to be formed, characterized in that the amorphizing implantation and said two implantations of dopants of opposite conductivity type are performed before the gate region is formed and at an angle with the surface of the semiconductor body which is substantially equal to 90 degrees.

2. (Previously presented) Method according to claim 1, characterized in that a first implantation of said two opposite conductivity type implantations is carried out using a first mask covering a first region of the semiconductor body and the second implantation of the two implantations is carried out after removal of the first mask, using a second mask of which the edge coincides with the edge of the first mask.

3. (Previously presented) Method according to claim 2, characterized in that the first mask and the second mask are formed in a self-aligned manner.

4. (Previously presented) Method according to claim 2, characterized in that the first mask is formed by a dummy gate region of a first dielectric material, and the first implantation is used to form the extensions of the source and drain regions.

5. (Previously presented) Method according to claim 4, characterized in that after the first implantation a uniform masking layer of a second dielectric material different from the first dielectric material is deposited on the semiconductor body and is subsequently removed by chemical mechanical polishing from the top of the dummy gate region which is then removed by selective etching, the remainder of the masking layer forming the second mask for the second implantation which is used to dope the neighboring part of the channel region.

6. (Previously presented) Method according to claim 5, characterized in that, after the second implantation, a uniform gate region layer is formed on top of the semiconductor body and is subsequently removed by chemical mechanical polishing from the top of the second mask which is then removed by selective etching.

7. (Previously presented) Method as claimed in claim 1, characterized in that the two implantations are annealed at a temperature between 500 and 700 degrees Celsius.

8. (Previously presented) Method as claimed in claim 1, characterized in that the source and drain regions are formed before the source and drain extensions.

9. (Previously presented) Method as claimed in claim 1, characterized in that for the amorphizing implantation ions are chosen from a group comprising Ge, Si, Ar or Xe.

10. (Previously presented) Method as claimed in claim 1, characterized in that a part of the function of the amorphizing implantation is provided by one of the two opposite conductivity type implantations.

11. (Previously presented) A semiconductor device comprising a field effect transistor obtained with a method as claimed in claim 1.

12. (Previously presented) A method of manufacturing a semiconductor device comprising:

providing a semiconductor body having a surface;

forming source and drain regions of a first conductivity type at the surface of the semiconductor body;

performing an amorphizing implantation to form an amorphized region in a region of the semiconductor body where a pn-junction is to be formed;

performing a first implantation of dopants of the first conductivity type, in at least part of the amorphized region where the pn-junction is to be formed, to form source and drain extensions of the first conductivity type;

performing a second implantation of dopants of a second conductivity type opposite the first conductively type, in part of the amorphized region where the pn-junction is to be formed, to form a channel region of the second conductivity type, the channel region extending between the source and drain extensions, thereby forming the pn junction;

forming a gate dielectric on the surface of the semiconductor body above the channel region formed in the amorphized region; and

forming a gate region on the gate dielectric.

13. (Previously presented) The Method according to claim 12, further comprising forming a first mask on a first region of the semiconductor body where the channel region is to be formed prior to performing the first implantation; forming a second mask on the semiconductor body after performing the first implantation, edges of the first mask coinciding with edges of the second mask; and removing the first mask prior to performing the second implantation, the second implantation being carried out using the second mask, and the amorphizing, first and second implants are performed at an angle with the surface of the semiconductor body that is substantially equal to 90 degrees.

14. (Previously presented) The Method according to claim 13, wherein the first mask and the second mask are formed in a self-aligned manner.

15. (Previously presented) The Method according to claim 13, wherein the first mask is formed by a dummy gate region of a first dielectric material.

16. (Previously presented) The Method according to claim 15, wherein the second mask is formed by depositing a masking layer of a second dielectric material, different from the first dielectric material, on the semiconductor body and subsequently removing, by chemical mechanical polishing, the second dielectric material from the top of the dummy gate region, the dummy gate region then being removed by selective etching prior to performing the second implantation.

17. (Previously presented) The Method according to claim 16, wherein the gate region is formed by depositing a gate region layer on top of the semiconductor body after performing the second implantation and subsequently removing, by chemical mechanical polishing, the gate region layer from the top of the second mask, the second mask then being removed by selective etching.

18. (Previously presented) The Method according to claim 12, further comprising annealing the first and second implantations at a temperature between 500 and 700 degrees Celsius.

19. (Previously presented) The Method according to claim 12, wherein the source and drain regions are formed before the source and drain extensions.

20. (Previously presented) The Method according to claim 1, wherein

initial portions of the source and drain regions are formed by an initial implantation carried out prior to the amorphizing implantation,

the amorphizing implantation is performed via an exposed upper surface of the semiconductor body of silicon, to form an amorphized region between the initial portions of the source and drain regions,

the first implantation of dopants is performed to form the extensions of the source and drain regions in the amorphized region and

the second implantation of dopants is performed to form a portion of the channel in the amorphized region, whereby the first and second implantations form a p-n junction in the amorphized region.